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APPLICATION NOTES

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HV Floating MOS-Gate Driver IC

(HEXFET is a trademark of International Rectifier)

by Steve Clemente and Ajit Dubhashi

Introduction

The gate drive requirements for a power MOSFET or IGBT utilized as a high side switch (drain connected to the high voltage rail, as shown in Figure 1) driven in full enhancement, i.e., lowest voltage drop across its terminals, can be summarized as follows:

1. Gate voltage must be 10-15V higher than the drain voltage. Being a high side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.

2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high side power device, which, in most applications, swings between the two rails.

3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

With these constraints in mind, several techniques are presently used to perform this function, as shown in principle in Table I. Each basic circuit can be implemented in a wide variety of configurations.

International Rectifier's IR2110 Gate Driver integrates most of the functions required to drive one high side and one low side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, the IR2110 provides very fast switching speeds (see Table II) and low power dissipation, and can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, the IR2110 driver can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz.

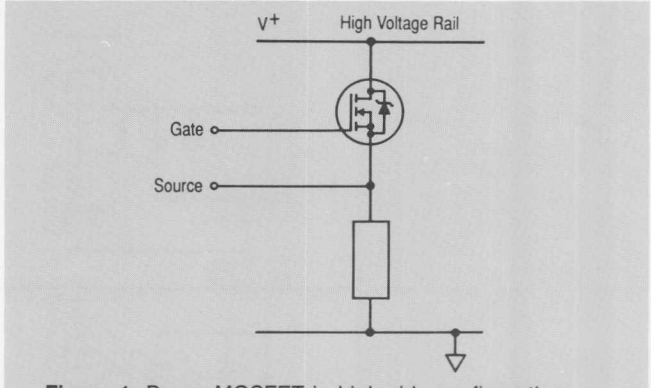


Figure 1. Power MOSFET in high side configuration

1. The Block Diagram of the IR2110

As shown in Figure 2, the IR2110 comprises a drive circuit for a ground referenced power transistor, another for a high side one, level translators and input logic circuitry.

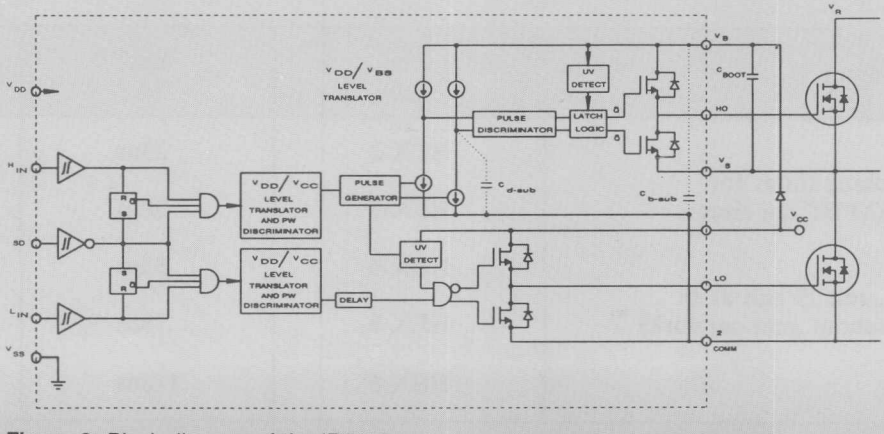


Figure 2. Block diagram of the IR2110

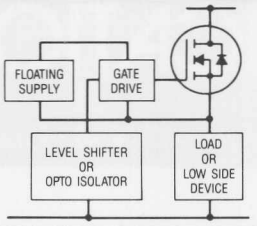
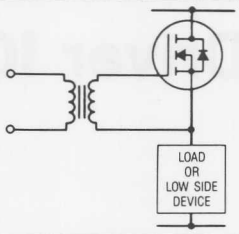
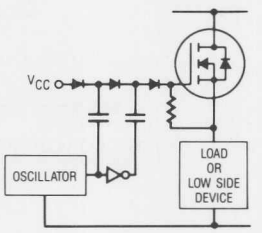
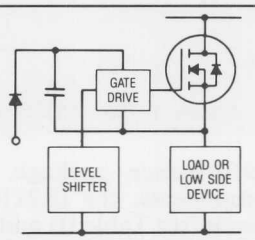
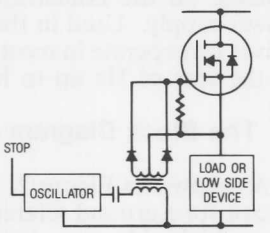
TABLE I		
METHOD	**BASIC CIRCUIT**	**KEY FEATURES**
FLOATING GATE DRIVE SUPPLY		Full gate control for indefinite periods of time. Cost impact of isolated supply is significant (one required for each high side MOSFET). Level shifting a ground referenced signal can be tricky: Level shifter must sustain full voltage, switch fast with minimal propagation delays and low power consumption. Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive.
PULSE TRANSFORMER		Simple and cost effective but limited in many respects. Operation over wide duty cycles requires complex techniques. Transformer size increases significantly as frequency decreases. Significant parasitics create less than ideal operation with fast switching waveforms.
CHARGE PUMP		Can be used to generate an "over-rail" voltage controlled by a level shifter or to "pump" the gate when MOSFET is turned on. In the first case the problems of a level shifter have to be tackled. In the second case turn on times tend to be too long for switching applications. In either case, gate can be kept on for an indefinite period of time. Inefficiencies in the voltage multiplication circuit may require more than two stages of pumping.
BOOTSTRAP		Simple and inexpensive with some of the limitations of the pulse transformer: duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. If the capacitor is charged from a high voltage rail, power dissipation can be significant. Requires level shifter, with its associated difficultiers.
CARRIER DRIVE		Gives full gate control for an indefinite period of time but is somewhat limited in switching performance. This can be improved with added complexity

Table II	**Die Size**	**Rise Time**	**Fall Time**
Typical switching times for different HEXFET die sizes (V_{CC} = 15V, test circuit as in Figure 9a, without gate network)	HEX-2	25ns	17ns
	HEX-3	38ns	23ns
	HEX-4	53ns	34ns
	HEX-5	78ns	54ns
	HEX-6	116ns	74ns

1.1 *Input logic*

Both channels are controlled by TTL/CMOS compatible inputs with transition thresholds proportional to the logic supply V_{DD} (3 to 20V) and Schmitt trigger buffers with hysteresis equal to 10% of V_{DD} to accept inputs with long rise time.

Each channel can be controlled independently from the other and the gate drive follows the input command within the limits of the propagation delay. In those applications where a deadtime is required to prevent conduction overlap in the power devices, the input commands have to be suitably spaced by the controlling logic. Section 4.3 shows a simple way to perform this function with few passive components.

The propagation delay between input command and gate drive output is approximately the same for both channels at turn-on (120ns) as well as turn-off (95ns) with a temperature dependence characterized in the data sheet.

The shutdown function is internally latched by a logic 1 signal and activates the turn off of both power devices. The first input command after the removal of the shutdown signal clears the latch and activates its channel. This latched shutdown lends itself to a simple implementation of a cycle-by-cycle current control, as exemplified in Section 4.3.

The signals from the input logic are coupled to the individual channels through high noise immunity level translators. This allows the ground reference of the logic supply (V_{SS} on pin 13) to swing by $\pm 5V$ with respect to the power ground (COM on pin 2). This feature is of great help in coping with the less than ideal ground layout of a typical power conditioning circuit. As a further measure of noise immunity, a pulse-width discriminator screens out pulses that are shorter than 50ns or so.

1.2 *Low Side Channel*

The output stage is implemented with two N-Channel MOSFETs in totem pole configuration (source follower as a current source and common source for current sinking), driven from the input circuits. Each MOSFET can sink or source gate currents of 2A. Because of the totem pole arrangement, the rise time of the gate waveform is slower than the fall time. This feature has a significant appeal in the great majority of power conditioning circuits. With clamped inductive loads, a slower turn-on reduces the peak reverse recovery current in the freewheeling diode with some increase in the turn-on losses. The full 2A sinking capability of the totem pole, on the other hand, gives good switching performance at turn-off, when most of the switching losses occur.

The source of the lower device in the totem pole is independently brought out to pin 2 so that a direct connection can be made to the source of the power device for the return of the gate drive current. The relevance of this will be seen in Layout Guidelines, Section 3.

An undervoltage lockout prevents either channel from operating if V_{CC} is below the specified value (8.6/8.2V). Any pulse that is present at the input when the UV lockout is released is forwarded to the appropriate channel.

1.3 *High side channel*

This channel has been built into an "isolation tub" (Figure 3) capable of floating from +500V to -5V with respect to power ground (COM on pin 2). The tub "floats" at the potential of pin 6 (V_S), which is established by the voltage applied to pin 5 (V_B). Typically this pin is connected to the source of the high side device, as shown in Figure 2 and swings with it between the two rails. If an isolated supply is connected between this pin and V_S (pin 6), the high side channel will switch the output (HO pin 7) between the positive of this supply and its ground in accordance with the input command.

One significant feature of MOS-gated devices is their capacitive input characteristic, i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current. If the high side channel is driving one such device, the isolated supply can be replaced by a capacitor, as shown in Figure 2. The gate charge for the high side MOSFET is provided by the bootstrap capacitor which is charged by the 15V supply through the bootstrap diode during the time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small.

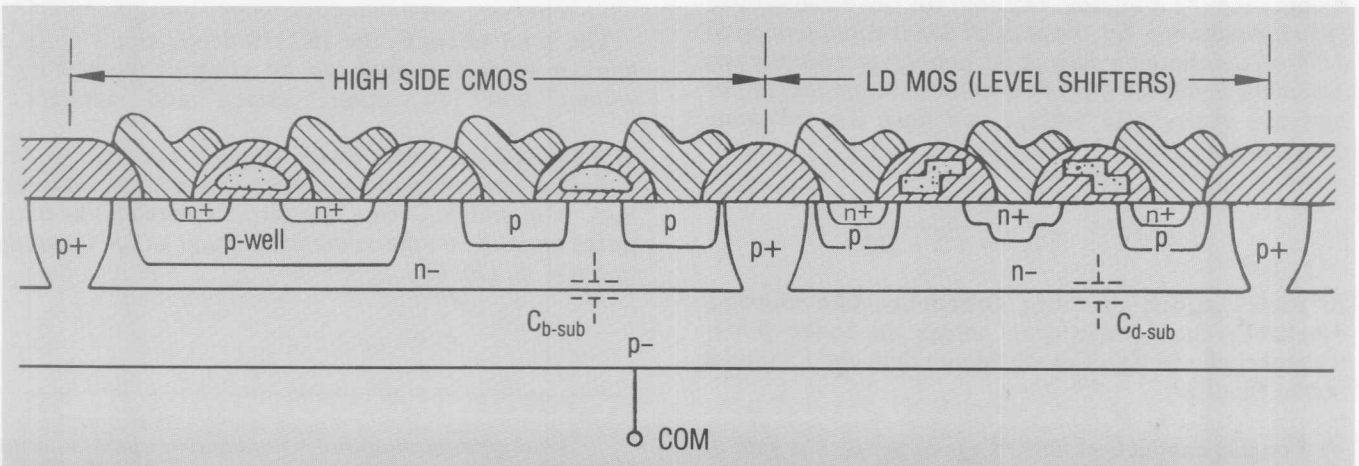


Figure 3. Silicon crossection showing the parasitic capacitances

The input commands for the high side channel have to be level-shifted from the level of COM to whatever potential the "tub" is floating at, which can be as high as 500V. As shown in Figure 2, the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential. The use of pulses greatly reduces the power dissipation associated with the level translation.

The pulse discriminator differentiates the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50V/ns in the power devices will not adversely affect the operation of the IR2110.

This channel has its own undervoltage lockout which blocks the gate drive if the voltage between V_S (pin 6) and V_S (pin 5), i.e., the voltage across the upper totem pole, is below its limits (8.7/8.3V). The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output.

The high voltage level translator circuit is designed to function properly even when the V_S node swings 5V below the COM pin. This can occur due to the forward recovery of the lower power diode or to the Ldi/dt induced voltage transient.

2. Application Guidelines

As shown in Figure 2, the bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines.

2.1 *The Bootstrap components*

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

a) Gate charge required (see also Ref. 1). After the turn-on charge has been delivered to the gate, the voltage across the bootstrap capacitor should be significantly higher than the minimum required for full enhancement (10V). Assuming, for the sake of illustration, a drop of 1.5V on the charging path of the bootstrap capacitor and assuming a voltage drop due to the internal leakage of half the excess gate voltage, we have the following constraint:

$$C_{BOOT} > \frac{2\ Q_G}{(V_{CC} - 1.5 - 10)}$$

In some unusual operating conditions, like transient overloads, the voltage drop across the lower power transistor can be significantly higher than the 1.5V used in the example.

b) Longest conduction time. The voltage on the gate of the power MOSFET at the end of the longest conduction time must be sufficient to keep it in full enhancement. The steady state current drawn from C_{BOOT} is equal to the quiescent current of the high side channel (I_{QBS}). Assuming the initial voltage calculated from the previous expression, this constraint translates into the following:

$$C_{BOOT} > \frac{2\ I_{QBS} \cdot t_{on}}{(V_{CC} - 1.5 - 1.0)}$$

c) Shortest conduction time. Stray impedances in the charging path limit the rate of charge of the bootstrap capacitor. Thus the capacitance should be low enough that the charge delivered to the gate plus the charge lost due to the quiescent current is totally replenished in the shortest conduction time for the lower power device. Conversely, a minimum conduction time may have to be maintained to insure that the bootstrap capacitor is fully charged.

d) Undervoltage lockout. If the voltage across the bootstrap capacitor falls below the undervoltage lockout threshold (8.3V) the power device is turned off and is kept off until the capacitor discharges to approximately 3.5V. Below this voltage the capacitor would not have enough charge to enhance the power device to any significant extent.

The value of 0.1 μF shown in Figures 6, 7 and 8 is adequate for a large die operated as low as 5kHz with a duty cycle close to 100 percent.

The bootstrap diode must be able to block the full voltage seen in the specific circuit; in the circuits of Figures 6, 7 and 8 this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100kHz it is approximately 12mA. The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason, it is important that this diode be ultra-fast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply.

2.2 *Power dissipation*

The total losses in the IR2110 driver result from a number of factors that can be grouped under "high voltage" and "low voltage," "static" and "dynamic."

a) Low voltage static losses ($P_{D(lv)q}$) are due to the quiescent currents from the three low voltage supplies, V_{DD}, V_{CC} and V_{SS}. In a typical 15V application these losses amount to approximately 3.5mW at 25°C, going to 5mW at 125°C[1].

[1] All temperatures mentioned in the text refer to junction, unless otherwise specified.

b) Low voltage dynamic losses ($P_{D(lv)sw}$) on the V_{CC} supply are due to two different components:

b1) Charge transfer to and from the gate of the power devices, i.e.,

$$P_G = 2V \cdot Q_G \cdot f$$

For two large IRF450 HEXFETs operated at 100kHz with V_{gs} = 15V, we have:

$$P_G = 2 \cdot 15 \cdot 120 \cdot 10^{-9} \cdot 100 \cdot 10^3 = 0.36W$$

The factor 2 in the formula is valid in the assumption that two devices are being driven, one per channel. If V_{SS} is generated with a bootstrap capacitor/diode, this power is supplied from V_{CC}. The use of gate resistors reduces the amount of gate drive power that is dissipated inside the IR2110 by the ratio of the respective resistances. The internal resistances are approximately 6 Ohms, sourcing or sinking, so that, if the gate resistor is 10 Ohms, only 6/16 of P_G is dissipated within the IR2110. These losses are not temperature dependent.

b2) Dynamic losses associated with the switching of the internal CMOS circuitry. They can be approximated with the following formula:

$$P_{CMOS} = V_{CC} \cdot Q_{CMOS} \cdot f$$

with Q_{CMOS} approximately equal to 16nC, largely independent from temperature. In a typical 100kHz application these losses would amount to 24mW.

c) High voltage static losses ($P_{D(hv)q}$) are mainly due to the leakage currents in the level shifting stage. They are dependent on the voltage applied on the V_S pin and they are proportional to the duty cycle, since they only occur when the high side power device is on. If V_S were kept continuously at 400V they would typically be 0.06mW at 25°C, going to 2.25mW at 125°C. These losses would be virtually zero if V_S is grounded, as in a push-pull or similar topology.

d) High voltage switching losses ($P_{D(hv)sw}$) comprise two terms, one due to the level shifting circuit (Figure 2) and one due to the charging and discharging of the capacitance of the high side p-well ($C_{b\text{-}sub}$ in Figure 3).

d1) Whenever the high side flip-flop is reset, a command to turn-off the high side device (i.e., to set the flip-flop) causes a current to flow through the level-shifting circuit. This charge comes from the high voltage bus through the power device and the bootstrap capacitor. If the high side flip-flop is set and the low side power device is on, a command to reset it causes a current to flow from V_{CC}, through the diode. Thus, for a half-bridge operating from a rail voltage V_R, the combined power dissipation is:

$$(V_R + V_{CC}) \cdot Q_P \cdot f$$

with Q_P the charge absorbed by the level shifter, and f the switching frequency of the high side channel. Q_P is approximately 5nC at V_R = 50V, going to 10nC as the rail voltage increases to 500V. In a typical 400V, 100kHz application these losses would amount to 0.375W. This includes the charging and discharging of $C_{d\text{-}sub}$. There is a third possible source for Q_P, when the high side flip-flop is being reset (i.e., the power device is being turned on) and the low side power device is off. In this case the charge comes from the high voltage bus, through the device capacitances and leakages or through the load. The power dissipation is somewhat higher than what would be calculated from the above expression.

In a push-pull or other topology where V_S (pin 5) is grounded, both level shifting charges are supplied from V_{CC} with significantly lower losses.

d2) In a high-side/low-side power circuit the well capacitance $C_{b\text{-}sub}$ is charged and discharged every time V_S swings between V_R and COM. Charging current is supplied by the high voltage rail through the power device and the epi resistance. Discharge occurs through the lower device and the epi resistance. The losses incurred in charging or discharging a capacitor through a resistor are equal to QV/2, regardless of the value of resistance. However, much of these losses occur outside the bridge driver, since the epi resistance is negligible compared to the internal resistance of the power devices during their switching transitions. Assuming a charge value of 9nC at 450V and an operating frequency of 100kHz, the *total* losses caused by the charging and discharging of this capacitance amount to:

$$Q \cdot V \cdot f = 9\ 10^{-9} \cdot 450 \cdot 10^5 = 0.4W$$

almost totally outside the IR2110. For all practical purposes, $C_{b\text{-}sub}$ cannot be distinguished from the output capacitance of the lower power device.

If V_S is grounded the capacitor is charged at a fixed voltage and these losses would be zero.

$C_{b\text{-}sub}$ (like $C_{d\text{-}sub}$) is a reverse biased junction and its capacitance is a strong function of voltage. For this reason, rather than giving the value in terms of capacitance, three charge values are given for three different voltages:

Voltage at V_S	Charge in $C_{b\text{-}sub}$
100V	3.3nC
200V	5.3nC
400V	9nC

These charges are not temperature dependent.

The above discussion on losses can be summarized as follows:

- The dominant losses are switching and, in high voltage applications at 100kHz or above, the static losses in Item a and Item c can be neglected outright.
- The temperature dependence of the switching losses is not significant;
- The combined losses are a function of the control mode, as well as the electrical parameters and temperature.

Knowing the power losses in the IR2110, the maximum ambient temperature can be calculated (and vice-versa) from the following expression:

$$T_{a\,max} = T_{j\,max} - P_D \cdot R_{th\,j\text{-}a}$$

where $R_{th\ j\text{-}a}$ is the thermal resistance from die to ambient. For the 14 pin DIL package this is 75°C/W maximum.

Figure 4 shows the power dissipation and the max ambient temperature at four different voltages when driving two IRF830 HEXFETs. Although measured in a specific set of operating conditions, these curves are general in nature and can be used to derive power losses and maximum ambient temperature for other operating conditions. To this end, the curve for $V_S = 0$ is of particular interest to isolate the low voltage components of losses since the high voltage ones become zero, as indicated above. The following example shows the breakdown of losses for operation of two IRF830 HEXFETs in a half-bridge from a 400V rail, 300kHz and no load:

$P_{D(lv)q}$ 0.004W

$P_{D(lv)sw}$: $P_{CMOS} = 15 \cdot 16 \cdot 10^{-9} \cdot 300 \cdot 10^3 =$ 0.072

$P_G = 2 \cdot 15 \cdot 28 \cdot 10^{-9} \cdot 300 \cdot 10^3 =$ 0.252

$P_{D(hv)q}$ 0.002

$P_{D(hv)sw}$: $(400 + 200) \cdot 9 \cdot 10^{-9} \cdot 300 \cdot 10^3 =$ 1.620

Total 1.950

Notice how the total is very close to the value shown in Figure 4a. The value of 200V in the formula to calculate $P_{D(hv)sw}$ is appropriate at no load, since this case would be the third in Section 2.2.d1.

If the power dissipation in the IR2110 turns out to be excessive for the maximum ambient temperature, the addition of external gate resistors decreases the amount of power dissipated inside the package (Item c), while keeping the combined gate dissipation constant. Switching losses may, in fact, increase.

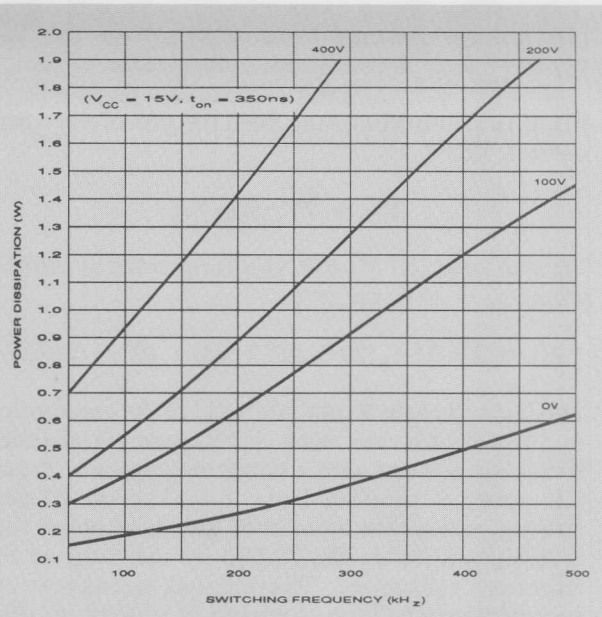


Figure 4a. Power dissipation as a function of frequency and operating voltage measured when driving two IRF830 HEXFET's in half-bridge configuration without gate resistors or load

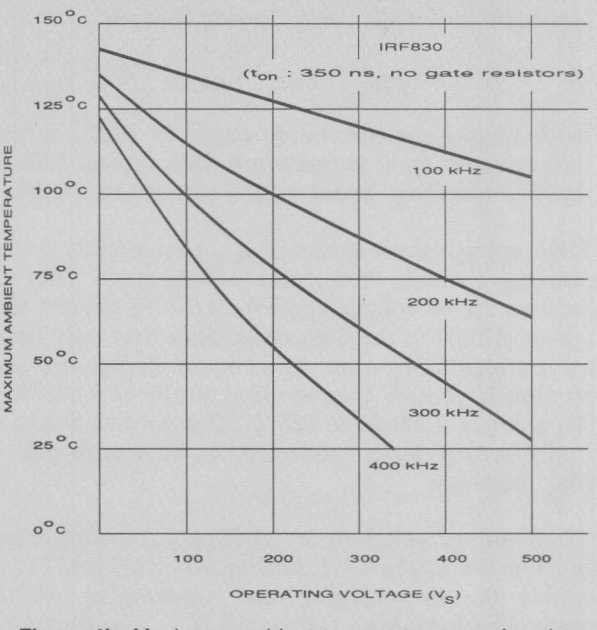


Figure 4b. Maximum ambient temperature as a function of frequency and operating voltage for half-bridge operation — This figure is derived from measured data, as shown in Figure 9a

The actual junction temperature can be measured while in operation by pulling 1mA from the Shutdown pin with the help of an adjustable current source, like the LM334. The voltage at the pin is 650mV at 25°C, decreasing by 2mV/°C.

3. Layout Guidelines

In spite of the noise immunity features mentioned in Section 1, great care should be exercised in the layout of

the power and control circuits to prevent false triggering and erratic operation. The following two areas require specific attention.

a) Stiffening the voltage busses.

Problems are normally encountered whenever logic and power meet. The IR2110 will be no exception, in spite of the precautions that have been taken in its design.

Because of the high di/dt frequently encountered in power circuits, any stray inductance in the power ground connections will cause voltage differentials to appear between the two ground pins and between COM pins of other IR2110s sharing the same power ground.

Particularly severe conditions of di/dt (hence, of ground noise) are encountered during commutation of the load current from the body drain diode of a MOSFET to the channel of another MOSFET. This second device will carry a large spike of reverse recovery current from the body drain diode of the previous MOSFET. For the duration of the reverse recovery significant Ldi/dt induced voltage transients will appear at the COM pin of the IR2110.

The peak of reverse recovery current is greatly reduced by slowing down the turn-on of the power MOSFET, while the problem of the voltage spike can be mitigated with good quality capacitors (low inductance and low ESR) between the two rails and compact assembly (Ref. 4, Figure 4).

To help the designers overcome these problems, the IR2110 is provided with two ground pins, V_{SS} (pin 13) and COM (pin 2) and has been designed to withstand $\pm 5V$ of transient offset between these two pins.

The pins, at opposite sides of the package, are *not* connected inside and an external connection is required. This connection can be directly between the two pins (Figure 6) or through a common ground (Figure 8), depending on the circumstances. As a general rule, V_{SS} should be used as a ground reference for the logic signals at the input and should be routed with them and with the logic supply V_{DD} (if different from V_{CC}), from wherever these signals are generated. COM, on the other hand, is mainly the gate return for the lower power device.

The routing of the power grounds, although not directly related to the operation of the IR2110, will affect its performance in terms of switching behavior and noise immunity. References 2 and 3 provide valuable guidelines and more detailed information on this subject and, specifically, on "how to minimize the noise voltage generated by currents from two or more circuits flowing through a common ground impedance."

Local decoupling capacitors should also be used to stiffen V_{CC} and V_{DD}. Both should be close to the pins of the IC and the bypass capacitor for the V_{CC} should be significantly larger than the bootstrap capacitor.

The potential discrepancy between V_{SS} and COM should be kept in mind when analyzing waveforms with an oscilloscope. The waveforms will be correct to the extent that the ground lead of the oscilloscope is short and tied to appropriate reference point. For example, if the gate waveform of the lower device is to be analyzed, the ground probe should be connected to the source pin of the device, and not to a generic "ground." In fact, it is useful to measure the noise voltage between one ground and another while switching high currents.

b) Gate charge/discharge loops.

The inductance of these loops should be minimized to reduce oscillations and to improve switching speed and noise immunity, particularly the "dv/dt induced turn-on" (Ref 4, Figure 2). To this end, each MOSFET should have a dedicated connection going to pins 2 and 5 of the IR2110 for the return of the gate drive signal. Best results are obtained with a twisted pair connected, on one side, to gate and source, on the other side, to gate drive and gate drive return. On pc boards parallel tracks should be used.

The use of gate resistors is a deviation from the general rule that gates should be driven from low impedance sources. This deviation is necessary, in most cases, for the following reasons:

- After all due care has been exercised, there still is an amount of inductance in the gate drive loop that causes unacceptable ringing.
- Switching speed of the power device needs to be slowed down for EMI considerations, particularly if its die size is small.
- The peak reverse recovery current needs to be reduced, as explained in Section 4.3 (see also Ref 5).
- The power dissipation in the IR2110 is excessive (Sections 2.2.b and d).

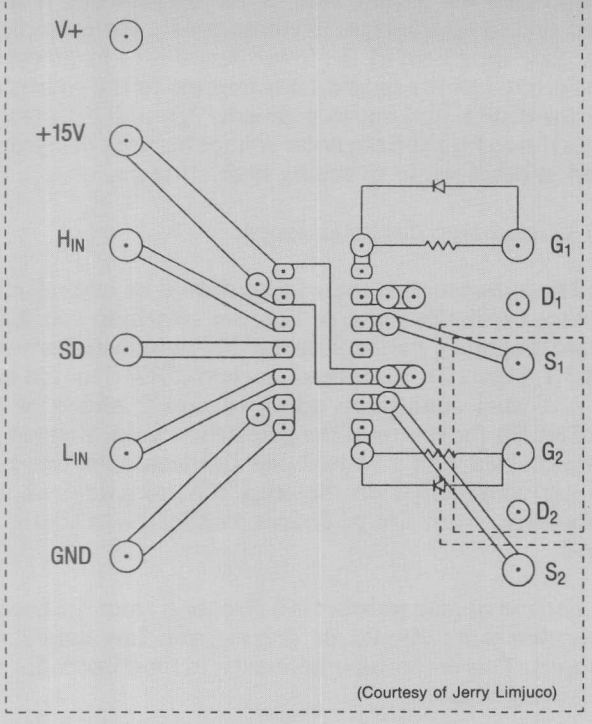
The layout shown in Figure 5a is a good vehicle to exemplify the impact of stray inductance in the gate drive loop. In this circuit the voltage differential measured between the gate pin of the power MOSFET and the drive pin of the IR2110 during a fast transient was in excess of 2V.

Figure 5b. shows an example of a compact layout for motor drives in the kW range.

4. Specific Applications

4.1 *Buck Converter*

Figure 6 shows a typical implementation of a buck converter with the high side drive function performed by the IR2110. The initial charge for the bootstrap capacitor comes from the V_{CC} supply through the inductor and the filter capacitor. The Q of this resonant circuit should be low enough to insure that the bootstrap capacitor does not get charged beyond the limits of V_{SS} (20V). If this is not so, a resistor in series with the bootstrap diode or a zener in parallel with the bootstrap capacitor would take care of possible overvoltages.



Note: Dotted lines represent pads on bottom side of board.
V+, GND, D_1, S_1, D_2, S_2, terminals have plated through holes

Figure 5a. IR2110 test circuit

If the converter is operated in the continuous current mode the bootstrap capacitor is charged during the conduction time of the freewheeling diode. In the discontinuous current mode, if the conduction time of the diode is very short, the charging of the bootstrap capacitor will be completed through the filter components and/or the load. This is true whether the dc-to-dc converter performs the function of a supply or speed control for a dc motor.

If the output voltage of the buck converter is between 10 and 20V, it can be used in place of a dedicated supply to power the PWM controller as well as the IR2110 and other auxiliary circuits. A start-up circuit is required to insure that the bootstrap capacitor is charged when power is first turned on. A resistor and diode from the rail voltage are commonly used for this purpose.

4.2 *Dual Forward Converter and Switched Reluctance Motor Drives*

Figure 7 shows a bridge arrangement that is frequently used to drive the windings of a switched reluctance motor. It is also known as a dual forward converter.

The use of the IR2110 requires the addition of three devices to insure that the bootstrap capacitor is charged at turn on and in subsequent cycles, should the conduction time of the freewheeling diodes become very short.

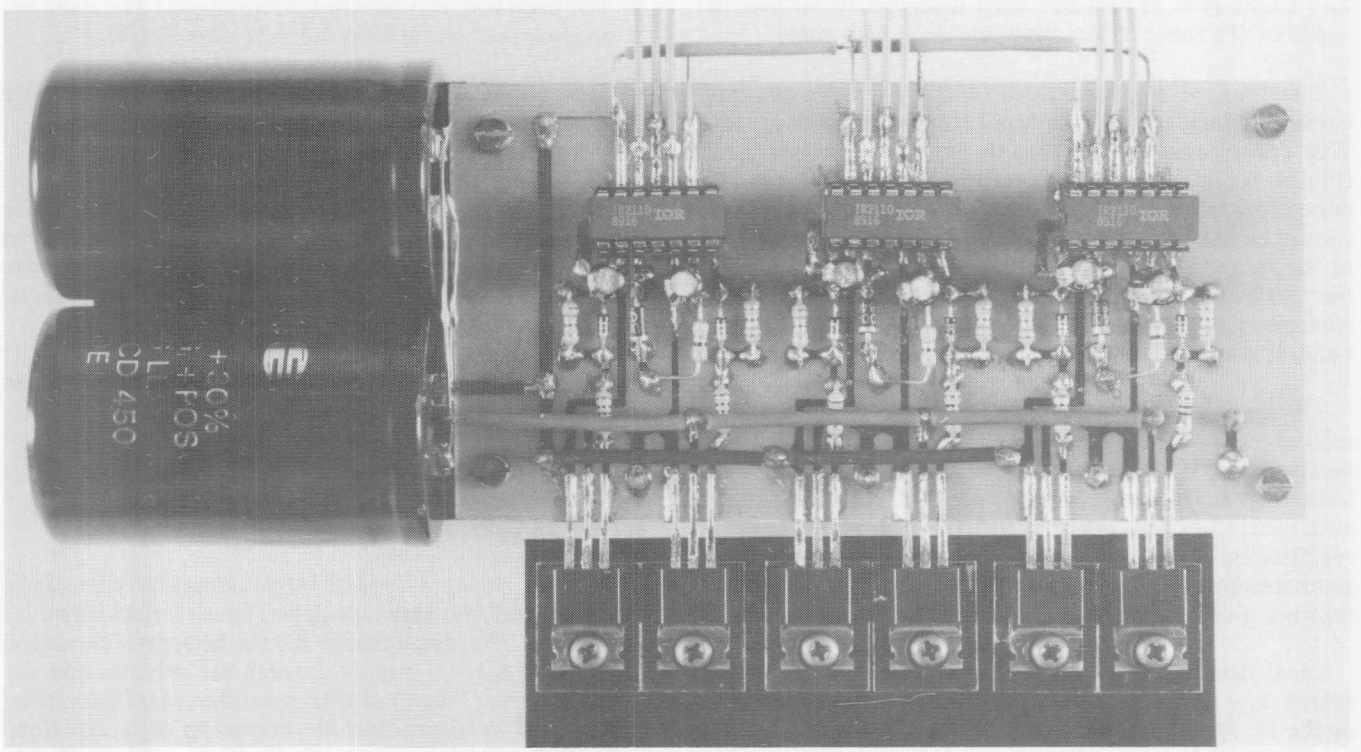


Figure 5b. Layout of a three-phase motor drive. The common ground point is the junction of the negative terminals of the reservoir capacitors. (Courtesy of Duncan Grant)

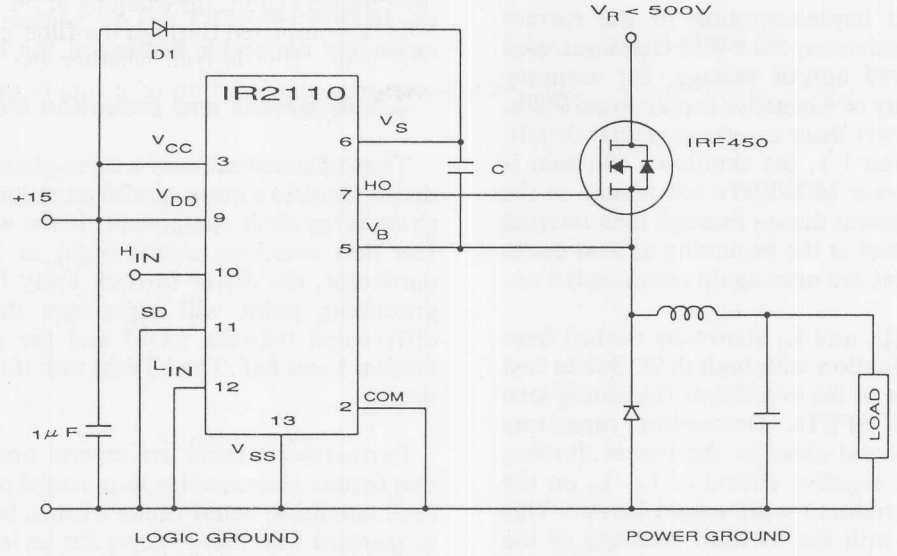


Figure 6. Buck Converter
Pins 11, 12, 13, 2 and the negative of the decoupling capacitor should be grounded together

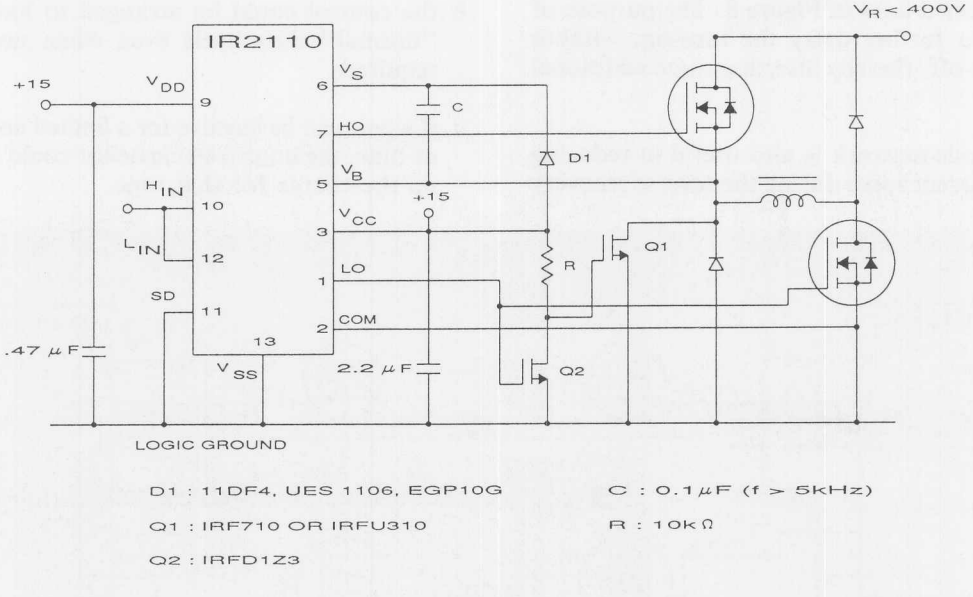


Figure 7. Dual forward converter and switched reluctance motors

4.3 *Full Bridge with Current Mode Control*

Figure 8 shows an H bridge with cycle-by-cycle current control implemented with current sensing devices on the low side in combination with the shutdown pin of the IR2110. The detailed implementation of the current sensing circuit is dependent on the PWM technique used to generate the desired output voltage, the accuracy required, the availability of a negative supply, bandwidth, etc. (Ref. 6, 7 and 8 cover these aspects in greater detail). As explained in Section 1.1, the shutdown function is latched so that the power MOSFETs will remain in the off-state as the load current decays through their internal diodes. The latch is reset at the beginning of next cycle, when the power devices are once again commanded on.

Stray inductances (L_1 and L_2 shown by dashed lines in Figure 8), in combination with high di/dt due to fast switching are the cause of the overshoots frequently seen across the power MOSFETs. Decoupling capacitors across the rail, connected close to the power devices, would cancel out the negative effects of L_1. L_2 on the other hand, must be reduced with a tight layout. This inductance, together with the forward recovery of the freewheeling diodes, causes the center point to swing outside of the rail voltage, i.e., V_S (pin 5) of the IR2110 would go below COM (pin 2). As mentioned in Section 1.3, this is allowed to -5V and erratic operation of the high side channel can occur if this limit is substantially exceeded.

The turn-on and turn-off propagation delays of the IR2110 are closely matched (worst case mismatch: 10ns), with the turn-on propagation delay 25ns longer than the turn-off. This, by itself, should insure that no conduction overlap of the power devices would occur, even if the on and off input command coincide. As an added safety margin a resistor diode network can be added to the gate, as shown with dashed lines in Figure 8. The purpose of this network is to further delay the turn-on, without affecting the turn-off, thereby inserting some additional dead-time.

The resistor-diode network is also useful in reducing the peak of the current spike during the reverse recovery time. As explained in Ref. 5, this has an impact on power losses, as well as dv/dt and EMI.

Figure 9 shows the waveforms taken from a test circuit laid out as shown in Figure 5a. Operation at 500kHz with the IRF830 HEXFET did not present any problem nor cause any noticeable heating of the IR2110.

4.4 *Brushless and Induction Motor Drives*

The implementation of a three-phase bridge for motor drives requires a more careful attention to the layout due to the large di/dt components in the waveforms and the fact that switching events occur at 120° intervals. In particular, the driver furthest away from the common grounding point will experience the largest voltage differential between COM and the ground reference. Section 3 and Ref. 2 and 3 deal with this subject in greater detail.

Furthermore, there are several operating conditions that require close scrutiny as potential problem areas. One such condition could occur when a brushless dc motor is operated with locked rotor for an indefinite period of time with one leg of the bridge being off. In this condition the bootstrap capacitor could eventually discharge, depending on the voltage seen by V_S during this period of time. As a result the top power device would not go on when commanded to do so. In most cases this would not be a cause for malfunction, since the lower device would be commanded on next and the bootstrap capacitor would be charged and ready for next cycle. In general, if the design cannot tolerate this type of operation, it can be avoided in one of three ways:

a. if the pole has been inactive for some time, the control logic turns on the lower device first;

b. the control could be arranged to have a very short "normal" duty cycle even when no conduction is required;

c. if a pole can be inactive for a limited and known period of time, the bootstrap capacitor could be sized to hold up the charge for that time.

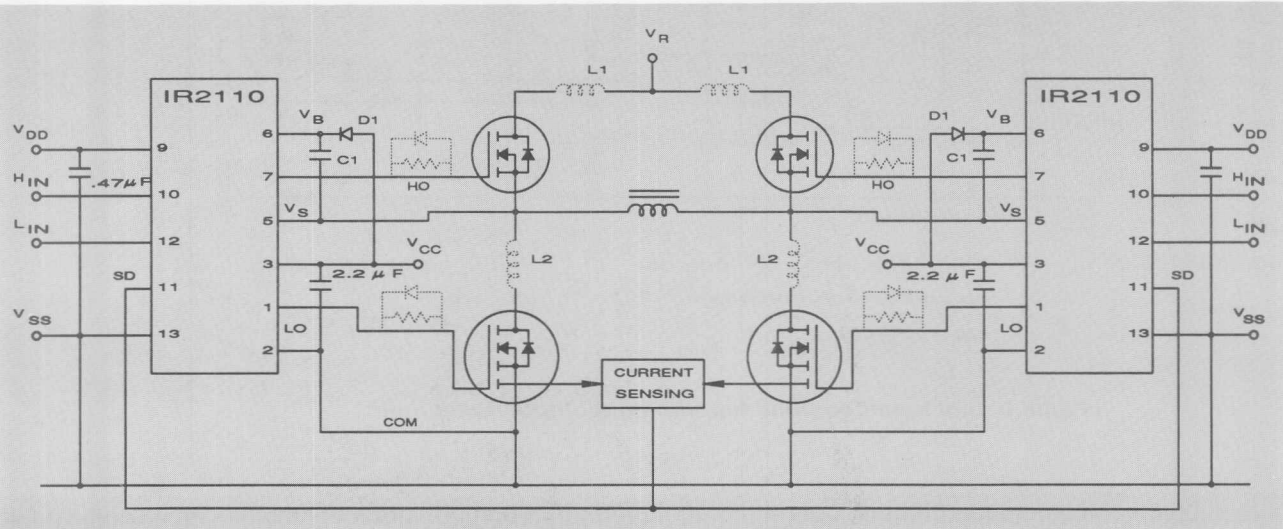


Figure 8. Typical implementation of all H bridge with cycle-by-cycle current mode control

If the bridge is part of an induction motor drive that use a PWM technique to synthesize a sine wave, each pole goes through prolonged periods of time with zero or very low duty cycle at low frequency. The bootstrap capacitor should be sized to hold enough charge to go through these periods of time without refreshing.

In circuits like the one shown in Figure 10, the isolation between the high voltage rail and the logic circuitry is supplied by the IR2110 as a reverse biased junction. A breakdown of one of these junctions would have disastrous consequences for the rest of the equipment. In many instances this cannot be allowed and some form of galvanic isolation is mandated by safety considerations or as a form of damage containment. Optoisolators or pulse transformers are frequently used to perform this function. The use of the IR2110 as a driver eliminates the dv/dt requirements that would otherwise be placed on these isolation components and reduces their cost while providing a high performance gate drive capability that is well beyond what these components perform directly.

4.5 *Push-Pull*

The IR2110 can still make a very useful contribution in applications that do not capitalize on its key feature, the high voltage level shifting and floating gate drive. Convenience, noise resilience between V_{SS} and COM and high speed drive capability are appealing features in most power conditioning applications. The IR2110 can perform the interface and gate drive function with the simple addition of two decoupling capacitors.

4.6 *High-Side P-Channel*

The IR2110 can also drive a P-Channel device as a high side switch, provided that a negative supply referenced to the positive rail is available, as shown in Figure 11. When operated in this mode, the H_{IN} input becomes active low, i.e. a logic 0 at the input turns on the P-Channel MOSFET.

Whenever V_S (or V_B) are at fixed potential with respect to ground, the power losses mentioned in Section 2.2.d.2 would be zero.

5. Troubleshooting Guidelines

To analyze the waveforms of the floating channel of the IR2110 a differential input oscilloscope is required. It is assumed that any voltage differential not referenced to ground is measured in this way.

It is also assumed that obvious checks have been made, for example:

- Pins are correctly connected and power supplies are decoupled.
- The bootstrap charging diode is ultra-fast, rated for the rail voltage.
- The shutdown pin is grounded.
- Logic inputs do not cause simultaneous conduction of devices, unless the topology requires it.

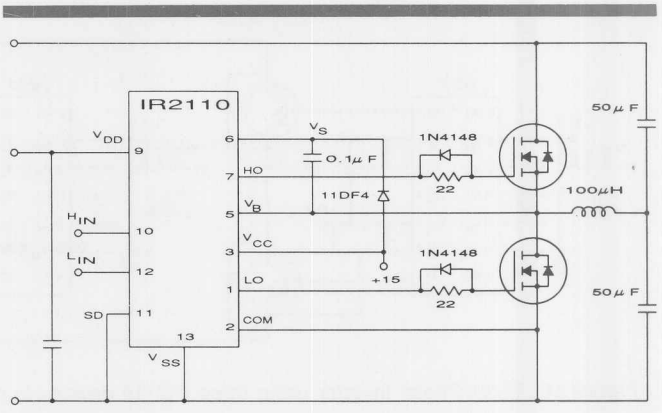


Figure 9a. Test circuit for waveforms shown below

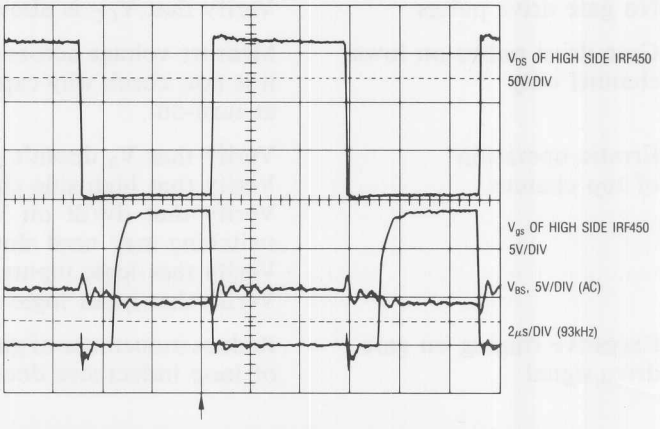


Figure 9b. Waveforms associated with the circuit shown in Figure 9a. IRF450 operated at approximately 100kHz in a 100 μH inductor.

The voltage drop across the bootstrap capacitor (0.1μF) due to the delivery of the gate charge is minimal (approx. 2V).

Due to the inductive nature of the load, the voltage across the HEXFET is close to zero even before gate voltage is present, because its internal diode goes in conduction when the other device goes off.

The resistor-diode network has the effect of slowing down the gate turn-on waveform substantially with minimal effect on the gate turn-off. In this particular operating mode the resistor-diode network does not perform a useful function because the turn-on occurs with zero volts across the HEXFET.

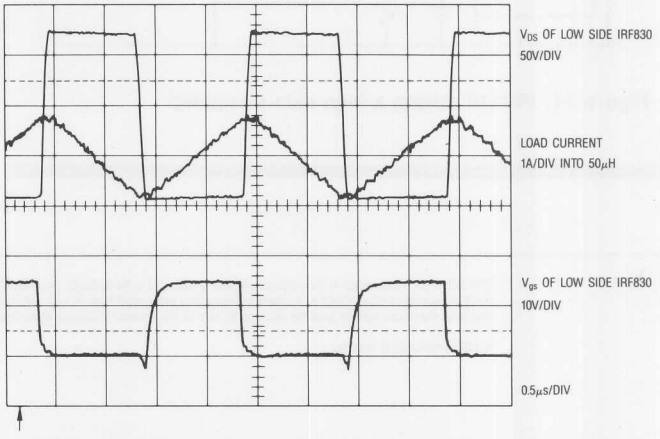


Figure 9c. Waveforms associated with the circuit in Figure 5a. IRF830's operated at 500kHz in a 50 μH inductor. The negative spike in the gate waveform is due to the forward recovery of the internal rectifier.

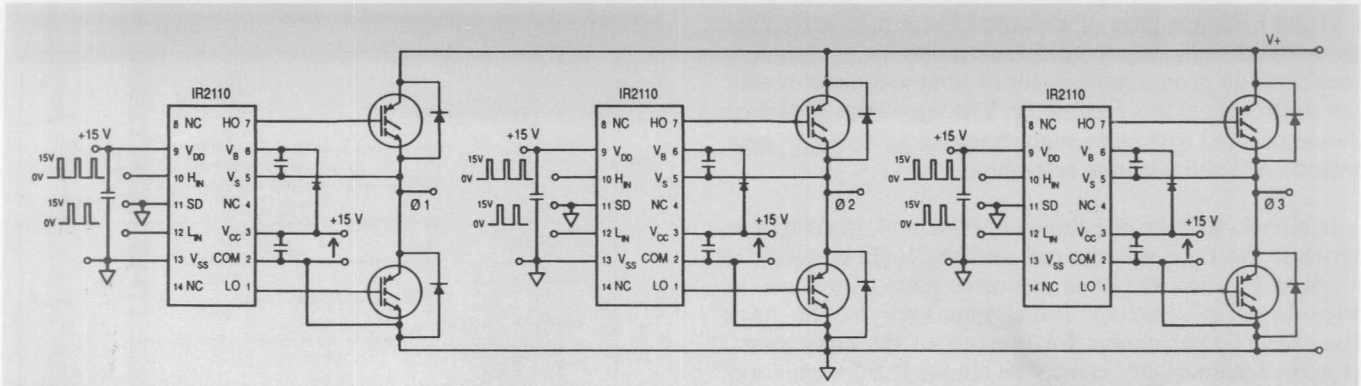


Figure 10. Three-Phase Inverter using three IR2110 devices to drive six IGBTs

SYMPTOM	POSSIBLE CAUSE
No gate drive pulses	Verify that V_{CC} is above the lockout level
Gate drive pulses on lower channel only	Measure voltage across bootstrap capacitor; it should be above the lockout level. If it is not, check why capacitor doesn't get charged. Insure that capacitor is charged at turn-on.
Erratic operation of top channel	Verify that V_S doesn't go below COM by more than 5V. Verify that high side channel does not go in undervoltage lockout. Verify that dv/dt on V_S with respect to COM does not exceed 50V/ns. If so, switching may need slowing down. Verify that logic inputs are noise-free with respect to V_{SS}. Verify that input logic signals are longer than 50ns.
Excessive ringing on gate drive signal	Reduce inductance of gate drive loop. Use twisted wires, shorten length. If reduction of loop inductance does not bring ringing to acceptable level, add gate resistors.

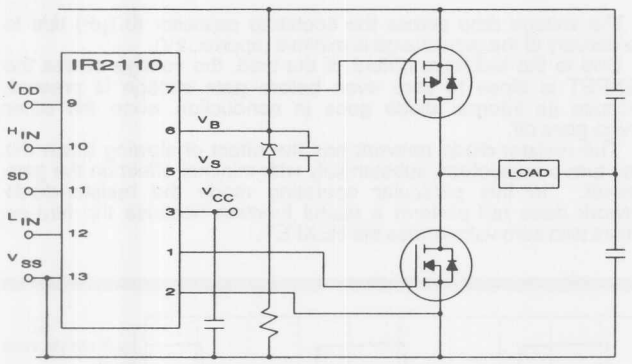


Figure 11. IR2110 driving a high side P-channel

References:

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3. "Noise Reduction Techniques in Electronic Systems" by H.W. Ott, John Wiley 1987
4. Application Note An-936 "The Do's and Dont's of using HEXFETs"
5. Application Note AN-967 "PWM Motor Drive with HEXFET III"
6. Application Note AN-961 "Using HEXSense in Current-Mode Control Power Supplies"
7. Application Note AN-959 "An Introduction to the HEXSense"
8. "Dynamic Performance of Current Sensing Power MOSFETs" by D. Grant and R. Pearce, Electronic Letters, Vol. 24 No. 18, Sept 1, 1988

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